

Massachusetts Institute of Technology

Center for Space Research

Room 37-521

mwb@space.mit.edu

11 March 2005

To: John Brinton
From: Mark Bautz, MIT Center for Space Research
Vyshnavi Suntharalingam, MIT Lincoln Laboratory
Subject: Annual report for NASA Grants NAG5-5401 and NDPR S-06566-G

The subject grants support development of High-Performance Active Pixel Sensors for X-ray Astronomy at the Massachusetts Institute of Technology (MIT) Center for Space Research and at MIT's Lincoln Laboratory. This memo reports our progress in the second year of the project, from April, 2004 through the present.

Goals & Overview

The purpose of this project is to use MIT Lincoln Laboratory's unique, silicon-on insulator (SOI) fabrication technology to produce an active-pixel X-ray imager with noise and spectral resolution comparable to state-of-the-art CCDs, but with orders of magnitude improvement in both readout rate and radiation tolerance. Such a sensor could be operated with much thinner optical blocking filters, and so would effectively have better soft-X-ray response than CCDs have. Finally, such a sensor might be able to operate at much higher temperatures than conventional CCDs, enabling lighter, simpler instruments with lower power consumption.

The project is organized into three phases. In the first phase, nearing completion at this writing, we have packaged and are characterizing a test active-pixel sensor (APS) designed and produced using internal Lincoln Laboratory funding. This sensor was intended as a design- and process-development device, and so is not expected to exhibit optimum X-ray detection performance. In phase two, which we began during year two of the project, we have been applying what we have learned from the test device to design a demonstration sensor that exhibits low noise and high readout rate. In phase three we plan to fabricate and test this demonstration sensor.

In the following two sections we summarize our work at MIT Center for Space Research (CSR) and at MIT Lincoln Laboratory(LL), and then briefly outline our plans for the coming year. In summary, we have developed test systems for testing at both the wafer-level (at LL) and packaged-part level (at CSR). The latter system is especially low-noise (about 3 electrons, RMS equivalent). We are using these test systems to characterize the amplifier responsivity, leakage current characteristics, and noise level of these devices. We have adapted a cryostat to allow low-temperature (-30C to -100C) testing of these devices, and expect to begin cold tests soon. We have considered a number of pixel designs for our next-generation sensor and we have identified one in the recent literature that will allow us to perform true correlated double sampling in each pixel. We have begun circuit simulations of this preferred design, and soon will begin detailed layout in preparation for a fabrication run that is expected to begin late in this

calendar year. Finally, we have identified a novel multi-wafer integration technology developed recently at Lincoln (the so-called 3-D architecture) which we plan to adopt for our next-generation device.

MIT Center for Space Research Activity Summary

MIT CSR's responsibilities include project direction and packaged device testing, and next-generation sensor design. We held seven team-wide meetings during the reporting period. A summary of our technical progress follows.

- **Test-system development:** The Astro-E2 electronics were successfully modified to provide the low-noise, differential-input video signal chain, CMOS-level biases, and various digital outputs required to operate packaged devices in both single-pixel and array format. We measured the electronics system noise by applying an (effectively) noiseless simulated detector signal train to the input and measuring the distribution of resulting digital output values. A representative histogram of these values is shown in Figure 1. The output pixel histogram is the stepped line; the smooth curve is the best-fit gaussian profile, which has a standard deviation of 2.8 digital channels. One channel corresponds to approximately one electron for an assumed sensor responsivity of 5 microvolts/electron. In addition, an existing cryostat was adapted for use with the APS sensors.
- **Packaged-device testing:** Both single-pixel and array-format devices were tested, and both showed sensitivity to visible light. Cooling the sensor to approximately -30C in the cryostat has been shown to reduce the dark current. The photo-diode pixels of the array-format devices are currently being tested with the low-noise signal chain. Results of this work will form part of the Master's thesis of MIT Electrical Engineering and Computer Science graduate student Matthew Cohen. Matt plans to submit his thesis in June, 2005.

MIT Lincoln Laboratory Activity Summary

MIT Lincoln Laboratories responsibilities include device packaging, wafer-level testing, and next-generation pixel design. Key accomplishments for the reporting period are:

- **Test-system development:** A Labview-based test system was developed to acquire test data on both single pixel structures and on the array. The system is currently configured for wafer-level testing, but could be used for packaged-device testing if need arises.
- **Wafer-level test results:** Both single-pixel and array format devices were tested at the wafer-level. Response to visible light was verified. A relatively large leakage current was detected through electro-static discharge (ESD) protection diodes on the array format devices, requiring as much as 30 mA from the VDDPG supply rail. The likely cause of this leakage has been identified and is not expected to be a serious problem in future production runs. Subthreshold (I_d - V_g), output (I_d - V_d), body-bias, and wafer-bias characteristics were measured on both n- and p-channel fully depleted SOI transistors.
- **Device Packaging:** "Development Lot" devices produced in year one were packaged to allow detailed characterization at MIT. Two package formats allowed testing of single-pixels and of complete arrays, respectively. Two devices were delivered to CSR in each format. See Figure 2
- **Transistor Model Development:** Using typical devices from a recent 350-nm gate length fabrication run, SPICE parameters were extracted from transistors with varying W/L

ratios. The model parameters fit into U.C. Berkeley's latest addition to BSIM -- BSIMSOI3.2, which properly captures the behavior of the floating body in fully depleted SOICMOS.

Design studies for a "Next Generation" X-ray APS Sensor at CSR and Lincoln

As proposed, this year we began design studies for a second-generation X-ray APS, which we call SOI/APS-2. CSR and Lincoln are working in very close collaboration on this effort. The team reviewed the literature on low-noise CMOS APS pixel designs, and selected one recently proposed by Kleinfelder and others (IEEE Transactions on Nuclear Science v 51, no. 5, p 2332, October, 2004) as a baseline line pixel design. The six-transistor design, shown schematically in Figure 3, which is excerpted from the Kleinfelder paper cited above, provides in-pixel correlated double sampling to minimize reset (kT/C) noise. This approach is particularly well-suited to the relatively large minimum pixel size (roughly 20 microns pitch or greater) required in typical X-ray imaging applications because the noise reduction factor is proportional to the square root of capacitance of C_2 in Figure 3. The large available pixel area can thus be exploited to minimize noise by maximizing the size of C_2 .

Using SPICE models of SOI transistors described above, we have begun simulations of the performance of this pixel design. Preliminary estimates suggests that a reset noise suppression by a factor of at least 10 should be possible within a 20 micron pixel. The simulations have also revealed the importance of self-heating of the transistors during readout.

In addition to a revised pixel design, we are also considering a novel device architecture, made possible by Lincoln's recently-developed "three-dimensional integrated circuit" (3-D) technology, for SOI/APS-2. This approach is described in a recent conference contribution by co-investigator Suntharalingam and others (IEEE Solid-State Circuits Conference 2005, paper 19.6). The 3-D technology allows the detection and analog processing functions to be assigned to separate silicon wafers. A unique, very dense wafer-to-wafer interconnection technology is used to integrate the two wafers. A visible-light imager fabricated from this technology (and described in the conference contribution cited above) features 1024x1024 pixels with 8 micron pixel pitch and with 2x2 micron vias connecting each pixel of the (photodiode) detector array on one wafer to the a corresponding active pixel readout circuit on another wafer.

The 3-D technology offers several potential advantages for future X-ray APS sensors. A very high optical fill-factor is possible because circuitry for each pixel can be placed below the corresponding detector. Back-illumination, which offers extended low-energy X-ray sensitivity, has been demonstrated in the visible with this technology. In principle, three or more layers can be integrated in a single device, allowing on-chip digitization and digital processing at very low power levels. A potential disadvantage of this technology is that, to date, no photo-gate detector layer has been demonstrated; photogate detectors may provide lower noise, and simpler readout timing, than photodiode detectors. We will evaluate these tradeoffs as we continue the design of SOI/APS-2.

Summary of Plans for Year Three

During the coming year we expect to complete noise and X-ray performance measurements for the various pixel designs incorporated in the SOI/APS-1 sensor. We expect to complete design and begin fabrication of the next-generation SOI/APS-2 sensor. As indicated in last year's progress report, we may not complete fabrication of SOI/APS-2 before the end of the third (and final) year of this program. In that event, we would expect to be able to complete characterization of this device if given a no-cost extension to the period of performance.

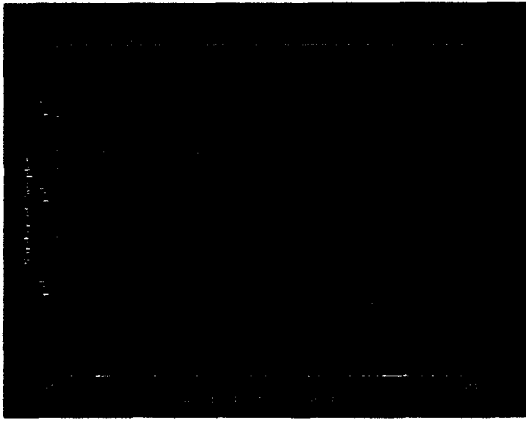


Figure 1: Noise histogram from CSR low-noise test electronics, obtained by applying a simulated 'noise-free' detector signal to the electronics input. The stepped (red) line is a histogram of observed digital output pixel values; the smooth curve is the best-fit gaussian, which has a standard deviation of 2.8 channels. For the expected APS sensor responsivity of 5 microvolts per electron, (about 1 electron per channel) the test electronics system noise is about 3 electrons.

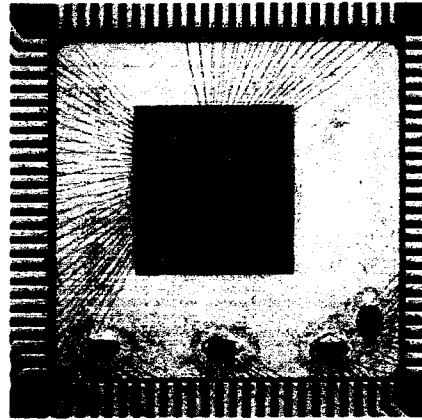


Figure 2: A packaged SOI/APS-1 device. The 256x256 pixel array and four single-pixel test structures have been included in this package. The packaged devices can be tested both at Lincoln and in CSR's low-noise test system.

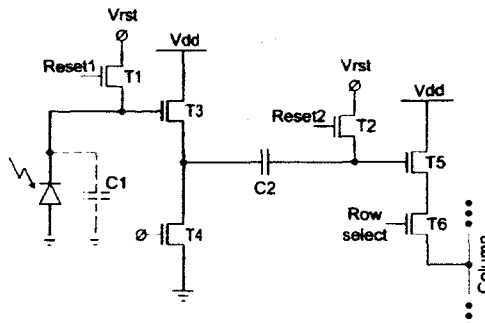


Figure 3: Schematic of a six-transistor, correlated-double sampling pixel design we are considering for our next-generation SOI/APS-2 device. The design is due to Kleinfelder et al. (2004 IEEE Trans. Nucl. Sci 51, 2332) and this figure is excerpted from Figure 11 of that work. Our preliminary simulations suggest that this design can provide a factor of ten reduction in reset noise if implemented in SOI CMOS in a 20-micron pixel.